Applying a Second-Generation Digital Audio Processor

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Optimod-FM Model 8200 is an all-digital transmission audio processor containing compression, high-frequency limiting, distortion-canceled clipping, and stereo generator functions. It is actually a computer that uses high-speed mathematical calculations to emulate these processing functions in real time. The calculations are performed by anywhere from six to nine Motorola 56001 digital signal processing chips, depending on the complexity of the processing system being emulated.

The 8200 is usually shipped with analog left and right inputs and outputs, plus a stereo encoder that provides an analog baseband output. It can also be fitted with AES/EBU digital inputs and outputs.

(Typical System configurations)

The first slide shows some typical transmission system configurations.

There are two types of digital I/O cards available. The first card accepts inputs with a 32kHz sample rate and frequency-locks the 8200's internal clock to this input. The digital output is also at 32kHz. Obviously, this card is limited to applications where the studio delivers low-jitter 32kHz digital audio to the processor, and where the STL or transmitter can accept 32kHz digital audio.

(Sample-rate converting digital I/O)

The second card is recently introduced, and contains two sample-rate converters — one for the input and one for the output. The next slide shows how this card works with the 8200 system. The AES/EBU receiver accepts any sample rate from about 30kHz to 50kHz. Depending on the input sample rate and the desired processing, the digital signal from the input receiver is either routed through the input sample-rate converter, or it is passed directly to the 8200 processing. If the input receiver detects a loss of digital input signal, it causes the 8200's analog inputs to become active.

One advantage of routing the input signal through a sample-rate converter chip is that the sample-rate converter automatically reduces any timing jitter in the input serial digital signal. This can potentially improve audio quality by eliminating any phase modulation of the clock in the audio processor. Such phase modulation could be passed to the processor's digital-to-analog converter and cause distortion sidebands to appear around the desired spectral components in the analog output.

If you only use the 8200's digital output, jitter reduction at the 8200's input may have no benefit if the device receiving the 8200's digital output is insensitive to jitter at its input.

The digital output from the 8200's processing is applied to a DSP chip, which performs several functions.

First, it realizes a digital output attenuator function, where it adjusts the scaling of the processed output signal with respect to the full-scale digital word.

Second, it can apply 50 or 75 microsecond de-emphasis to the digital signal, so that the digital output can be either flat or pre-emphasized.

Third, it can apply a J.17 pre-emphasis to the signal, which is useful in NICAM STLs or on-air transmission.

Finally, it can determine if the output word length is 14 bits or 18 bits, and it re-dithers the signal to prevent distortion at low levels.

If the desired output sample rate is different than 32kHz, the output of the DSP chip is routed through the output sample-rate converter. Finally, it is applied to the AES/EBU transmitter.

(Sample-rate converter operating modes)

There are five distinct operating modes available from the sample-rate converting digital I/O board. The first three take any input sample rate, and output 32kHz, 44.1kHz, or 48kHz.

The fourth locks the output sample rate to the input sample rate, and is useful in plants where the sample rates of all digital devices are locked to house sync.

The fifth is a locked three-to-two divider. It accepts a 48kHz input signal and outputs a 32kHz signal that is frequency-locked to the 48kHz input in a three-to-two relationship. It is used in plants where the studio sample rate is 48kHz, while the long-haul transmission sample rate is 32kHz.

(House sync digital audio processing in genlocked environment)

This diagram shows another application of the sample-rate converting digital I/O card. In this application, the actual audio input is analog, and the digital input is used only for house sync. The house sync can be at either 32kHz or 48kHz, and the genlocked digital output can also be at either 32kHz or 48kHz. The card supports any combination of these frequencies.

(Sample-rate converter output pre-emphasis)

The card's on-board DSP accommodates almost any system pre-emphasis requirement. The most common application requires the digital output to be pre-emphasized at either 50 or 75 microseconds. This depends on the pre-emphasis used by the earlier digital audio processing. This signal is tightly peak-controlled to 100% modulation, and is applied directly to a stereo generator with an AES/EBU digital input.

Sometimes, the system following the audio processor applies its own 50 or 75 microsecond pre-emphasis. In this case, the DSP in the sample-rate converter digital I/O card applies a very accurate 50 or 75 microsecond de-emphasis in the digital domain. This de-emphasis emulates both the magnitude and phase response of an analog RC rolloff. Since the magnitude and phase of the following pre-emphasis is unlikely to exactly complement this rolloff, this arrangement may cause a small amount of peak overshoot, and it should only be used if you can't turn off the pre-emphasis in the device receiving the 8200's output.

Particularly in Europe, a significant number of digital STLs use NICAM encoding with J.17 pre-emphasis. J.17 is an upward-shelving pre-emphasis with breakpoints at approximately 400Hz and 4kHz. There is also a digital sound system for television that multiplexes a J.17 pre-emphasized NICAM signal onto the video carrier. These systems require the audio processor to apply J.17 pre-emphasis in the digital domain.

It is common for the analog outputs of a NICAM STL receiver to feed a conventional FM exciter with built-in 50 or 75 microsecond pre-emphasis. In this case, the audio processor has to high-frequency-limit the signal to 50 or 75 microseconds. Then it applies the 50 or 75 microsecond de-emphasis to the signal before the signal is applied to the NICAM digital STL. Of course, you also have to apply the J.17 pre-emphasis. A diagram should make this clearer.

(Application of combined J.17 and 50 microsecond pre-emphasis.)

Here we have an 8200 driving a NICAM STL with a digital input. The NICAM decoder turns the signal into analog and applies J.17 de-emphasis. The analog signal is applied to the FM exciter.

If you are able to defeat the pre-emphasis in the exciter, you don't need to apply 50 microsecond de-emphasis digitally in the audio processor. This scenario creates the most accurate peak modulation control.

However, many large networks in Europe use standardized transmitters that apply 50 microsecond pre-emphasis. In this case, of course, you have to apply de-emphasis digitally in the audio processor.

(8200 system block diagram)

In the time remaining, let me show you a block diagram of what goes on inside our digital audio processor. There are two very low-noise instrumentation amplifiers that receive the left and right analog inputs. The amplifiers' gains can be digitally programmed in approximately 2dB steps over a 26dB range. We determine the drive level into the following analog-to-digital converter by setting this gain, so that we always use as much of the dynamic range of the A-to-D as we possibly can.

The mainframe can accommodate up to four DSP boards. Each board contains three Motorola 56001 DSP chips, along with circuitry that lets the chips communicate among themselves at high speed. The basic two-band and protection processing structures use two boards, and the five-band structure uses three boards. Our new television processor is based on the 8200 mainframe and uses all four boards because it permits dual-mono operation of its processing structures.

The first board receives the 18-bit digital data from the A-to-D converter or the AES/EBU digital interface card. As the data is processed, it is passed sequentially from one DSP board to the next. When all of the processing is done, the processed data is passed to the 18-bit digital-to-analog converter, and also to the AES/EBU digital output interface.

The stereo analog outputs of the D-to-A converter are passed to a pair of 8-bit multiplying D-to-A converters, which determine the output level of the analog signal independently of the output level of the AES/EBU digital signal. If you need to have the analog outputs "flat," the necessary de-emphasis is performed in the analog domain.

The output of the reconstruction filters also drive the stereo encoder. This is a very high-quality analog circuit that generates the stereo baseband by first matrixing the signal into sum and difference components. The difference component is applied to two sets of analog switches that operate at 38kHz and 114kHz respectively, using switching waveforms called "Walsh functions." When the outputs of these switches are summed in correct proportion, all frequency components up to 251 kHz are theoretically cancelled. This makes the design of the baseband low-pass filter somewhat easier. However, due to imperfections in real-world circuitry, these components are not completely canceled, so our baseband low-pass filter actually starts rolling off at 70kHz, and is almost 20dB down at 114kHz, which is the third harmonic of 38kHz. This provides an extremely clean baseband above 100kHz.

To improve potential separation even more, the baseband low-pass filter is phase-corrected. The theoretical separation for this filter design exceeds 70 dB from 30 to 15 thousand Hertz.

The entire system is digitally controlled by a Z-180 8-bit microprocessor. This micro handles incoming data on the RS-232 interface and also on the 8 programmable optically-isolated binary inputs. With the help of

a little external logic, it reads the seven front-panel pushbutton switches and the rotary encoder. It provides information to be shown on the front-panel LCD display, including real-time representations of gain reduction and level meters. It supervises the real-time clock, and can synchronize the clock to the incoming AC line frequency. And of course it loads DSP code into the 56001s to determine the audio processing structures that the 56001s emulate. The code also determines the control settings inside those structures.

So there you have it. The 8200 is basically a very fast real-time computer under the control of a much slower computer that does the housekeeping. The whole thing is programmed in assembly language to get maximum speed from the hardware. For example, booting up from a cold start takes less than a second, and you can change a processing structure in about 50 milliseconds. Since it's a computer, the 8200 is entirely under software control, so improvements and updates require only that you replace a read-only-memory module.

The all-digital signal path is one building block in the all-digital radio station of the near future. With the availability of moderate-cost sample-rate converter ICs, the system can operate either synchronously or asynchronously to the digital plant's master clock, and can interface to any sample rate in common professional use.